
 OSTİM TEKNİK ÜNİVERSİTESİ A N K A R A	FACULTY OF ENGINEERING COURSE SYLLABUS FORM	Doküman No	MF.FR.003
		Revizyon Tarihi	13.11.2024
		Revizyon No	01
		Sayfa No	1 / 6

EEE 303 – DIGITAL SYSTEM DESIGN				
Course Code	Course Name		Semester	
EEE 303	Digital System Design		Fall <input checked="" type="checkbox"/> Spring <input type="checkbox"/> Summer <input type="checkbox"/>	
Hours			Credit	ECTS
Theory	Practice	Lab	3	5
3	0	0		


Course Details	
Department	Electrical and Electronics Engineering
Course Language	English
Course Level	Undergraduate <input checked="" type="checkbox"/> Graduate <input type="checkbox"/>
Mode of Delivery	Face to Face <input checked="" type="checkbox"/> Online <input type="checkbox"/> Hybrid <input type="checkbox"/>
Course Type	Compulsory <input checked="" type="checkbox"/> Elective <input type="checkbox"/>
Lecturer(s)	Dr. Şenol Gülgönül
Course Objectives	<p>Understand the Fundamentals: Gain a solid understanding of digital system design principles and the role of Hardware Description Languages (HDLs) in the design process.</p> <p>Master Verilog HDL: Develop proficiency in Verilog HDL for modeling, designing, and simulating digital systems.</p> <p>Design Combinational and Sequential Circuits: Learn to design and implement both combinational and sequential logic circuits using Verilog HDL.</p> <p>Implement Digital Systems: Apply Verilog HDL to design, simulate, and verify complex digital systems, including finite state machines.</p> <p>Utilize FPGA Technology: Gain hands-on experience with FPGA technology and tools for implementing digital designs.</p> <p>Develop Testbenches: Create and use testbenches to verify the functionality and performance of digital designs.</p>

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Course Content	<ul style="list-style-type: none"> • Gate Level Modeling and Testbench • Data Flow Modeling • Behavioral Modeling • Sequential Logic Circuits Using Verilog • Verilog and FPGA Implementation • Microcontroller Architecture
Course Method/ Techniques	Lecture <input checked="" type="checkbox"/> Question & Answer <input type="checkbox"/> Presentation <input type="checkbox"/> Discussion <input type="checkbox"/>
Prerequisites/ Corequisites	
Work Placement(s)	
Textbook/ References/ Materials	
<ul style="list-style-type: none"> • Digital Design Global Edition by Morris Mano and Micheal Ciletti 	

Course Category				
Mathematics and Basic Sciences	<input checked="" type="checkbox"/>		Education	<input type="checkbox"/>
Engineering	<input checked="" type="checkbox"/>		Science	<input checked="" type="checkbox"/>
Engineering Design	<input checked="" type="checkbox"/>		Health	<input type="checkbox"/>
Social Sciences	<input type="checkbox"/>		Profession	<input checked="" type="checkbox"/>

Weekly Schedule		
No	Topics	Materials/Notes
1	Introduction	Chapter - 3
2	Simulation and Waveforms	Chapter - 3
3	Gate Level Modeling	Chapter - 3
4	Testbench	Chapter - 4
5	Data Flow Modeling	Chapter - 4
6	Combinatorial Circuits Design	Chapter - 4
7	Review	
8	Midterm Exam	
9	Behavioral Modeling	Chapter – 5


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10	Sequential logic circuits using Verilog	Chapter - 5
11	FPGA Introduction	Chapter – 7
12	FPGA Applications	Chapter – 7
13	Finite State Machines	Chapter – 8
14	Microcontroller Architecture	Chapter - 8
15	Review	
16	Final Exam	

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Assessment Methods and Criteria		
In-term studies	Quantity	Percentage
Attendance		
Lab		
Practice		
Fieldwork		
Course-specific internship		
Quiz/Studio/Criticize		
Homework		
Presentation / Seminar		
Project	1	20%
Report		
Seminar		
Midterm Exam	1	20%
Final Exam	1	60%
Total		100%
Contribution of Midterm Studies to Success Grade	1	40%
Contribution of End of Semester Studies to Success Grade	1	60%
Total		100%

ECTS Allocated Based on Student Workload			
Activities	Quantity	Duration (Hrs)	Total Workload
Course Hours	16	3	48
Lab			
Practice			
Fieldwork			
Course-specific Work Placement			
Out-of-class study time	16	5	80
Quiz/Studio/Criticize			
Homework			
Presentation / Seminar			
Project	1	50	50
Report			
Midterm Exam and Preparation for Midterm	1	23	23
Final Exam and Preparation for Final Exam	1	24	24
Total Workload			225
Total Workload / 25			9
ECTS Credit			5

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Course Learning Outcomes	
No	Outcome
L1	Understand Digital Design Principles
L2	Develop Verilog HDL Skills
L3	Design and Implement Digital Systems
L4	Create Effective Testbenches
L5	Apply FPGA Technology


Contribution of Course Learning Outcomes to Program Competencies/Outcomes															
<i>Contribution Level: 1: Very Slight, 2: Slight, 3: Moderate, 4: Significant, 5: Very Significant</i>															
	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11				Total
L1	5	5	5	5	5	5	5	5	4	4	4				-
L2	5	5	5	5	5	5	5	5	4	4	4				-
L3	5	5	5	5	5	5	5	5	4	4	4				-
L4	5	5	5	5	5	5	5	5	4	4	4				-
L5	5	5	5	5	5	5	5	5	4	4	4				-
Total															-

i. Sufficient knowledge in the fields of mathematics, natural sciences, and related engineering disciplines; the ability to apply theoretical and practical knowledge in solving complex engineering problems.

ii. The ability to identify, formulate, and solve complex engineering problems; the ability to select and apply appropriate analysis and modeling methods for this purpose.

iii. The ability to design a complex system, process, device, or product to meet specific requirements under realistic constraints and conditions; the ability to apply modern design methods for this purpose.

iv. The ability to select and use modern techniques and tools required for the analysis and solution of complex problems encountered in engineering applications; the ability to effectively use information technologies.

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v. The ability to design experiments, conduct experiments, collect data, analyze results, and interpret findings for the investigation of complex engineering problems or discipline-specific research topics.

vi. The ability to work effectively in intra-disciplinary and multidisciplinary teams; the ability to work independently.

vii. The ability to communicate effectively both orally and in writing; proficiency in at least one foreign language; the ability to write effective reports, understand written reports, prepare design and production reports, make effective presentations, and give and receive clear and understandable instructions.

viii. Awareness of the necessity of lifelong learning; the ability to access information, track developments in science and technology, and continuously renew oneself.

ix. Acting in accordance with ethical principles, knowledge of professional and ethical responsibilities, and the standards used in engineering applications.

x. Knowledge of business practices such as project management, risk management, and change management; awareness of entrepreneurship and innovation; knowledge of sustainable development.

xi. Knowledge of the impact of engineering practices on health, environment, and safety at global and societal levels, and awareness of contemporary engineering issues; awareness of the legal consequences of engineering solutions.